CMOS image sensors for machine vision in the era of artificial intelligence

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Organized by projects: 2020005 Mantis Vision (Penta)
2021004 Imagination (Penta)
2023022 Elevation (Xecs)

Outline

- Machine vision
- Key requirements and technology enablers for image sensors in machine vision
- What's next? Can we make our pixels more "artificially" intelligent

Add photo race zelfrijdende autotjes.

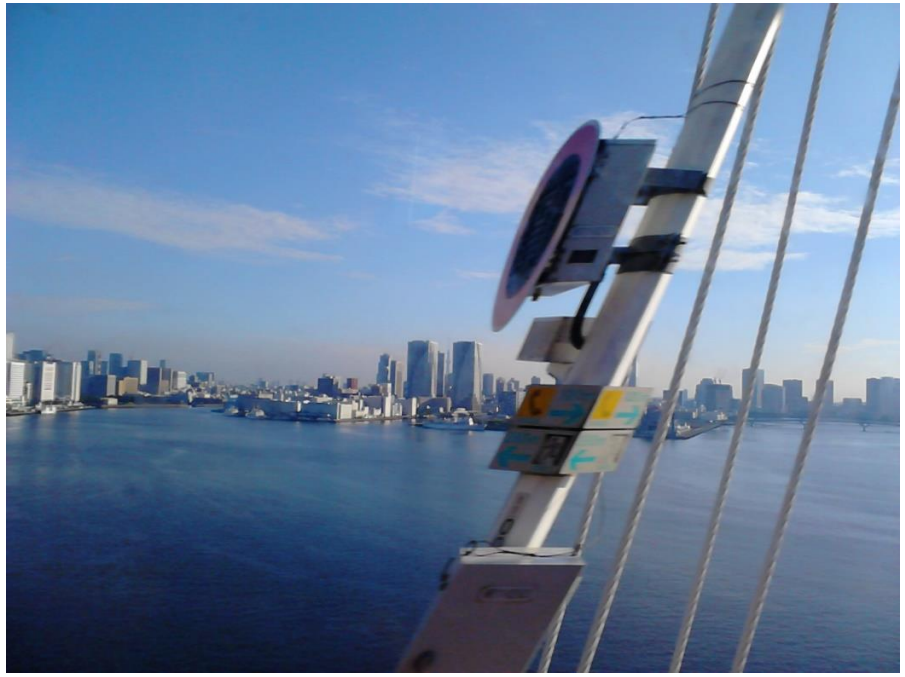
Machine vision

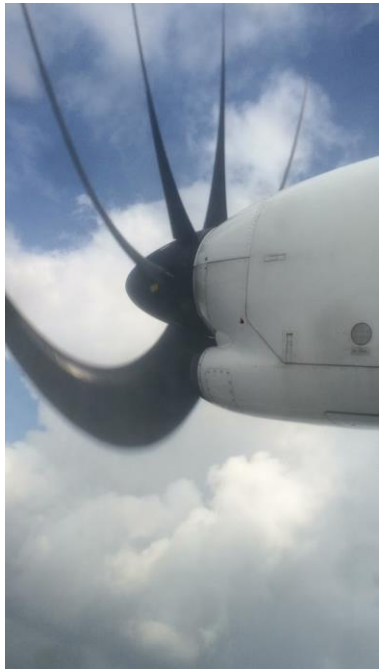
- The ability of a machine to see, to use vision to take decisions
  - Automatic inspection
  - Process control
  - Autonomous navigation and robot control
- Interdisciplinary engineering discipline
- Related to computer vision
  (a computer science discipline)



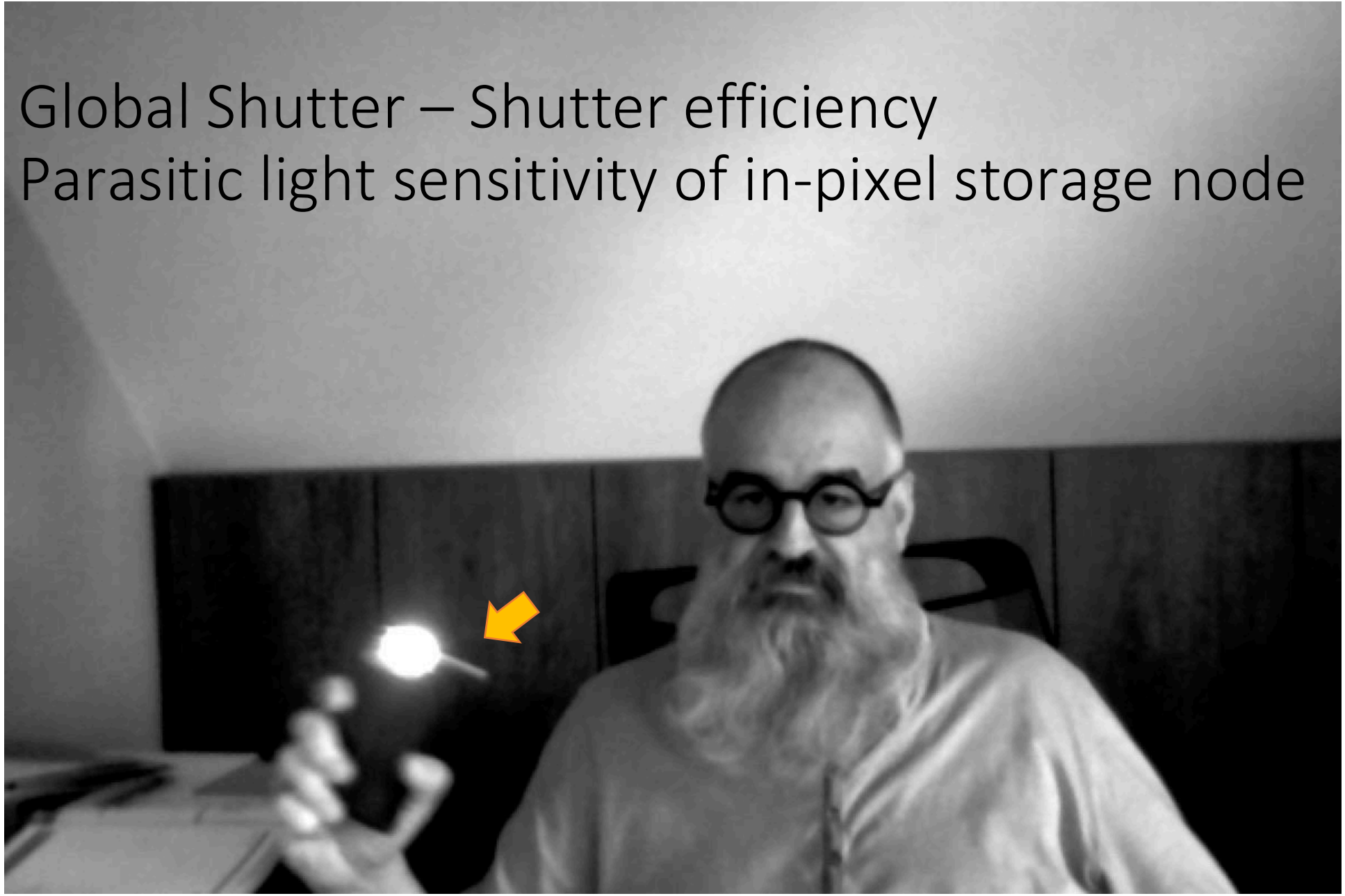

Machine vision needs

- Image should be a true represenation of the environment





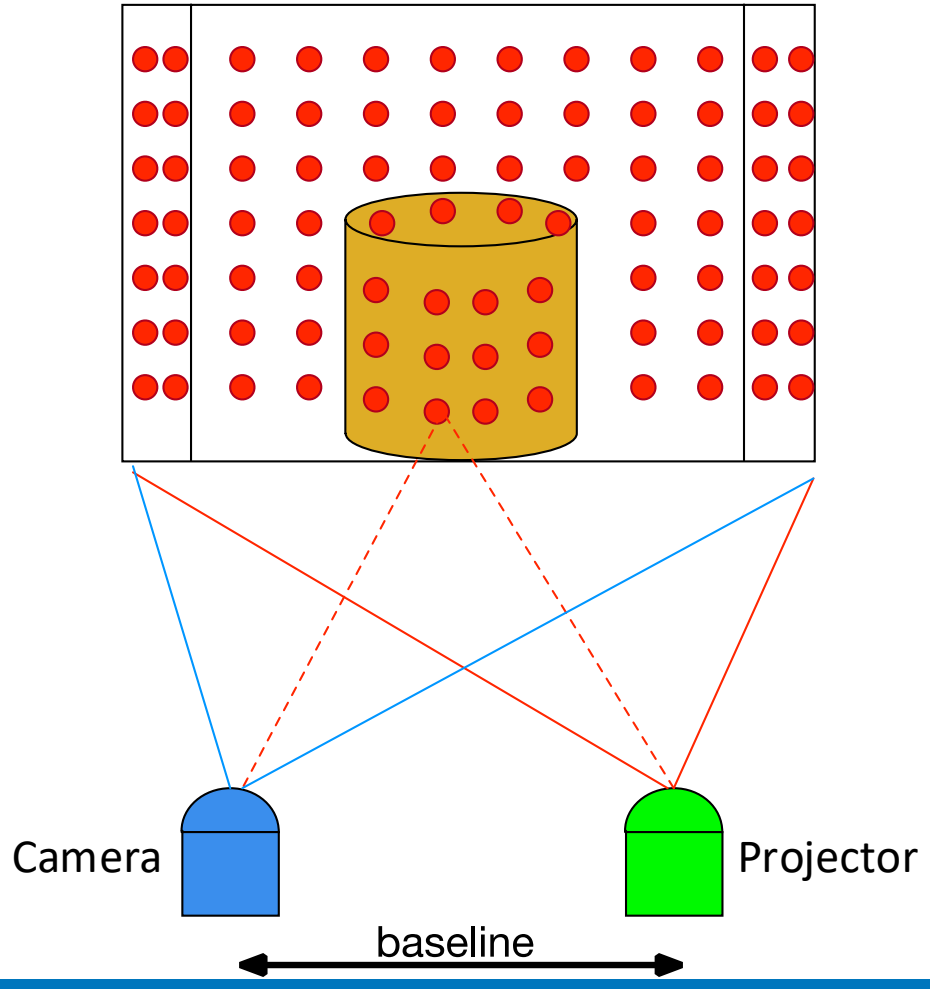
Global Shutter – Shutter efficiency
Parasitic light sensitivity of in-pixel storage node



Machine vision requirements mapping on image sensor requirements

Issue	Solution	Camera	Image Sensor
Motion blur	Short exposure time	High light sensitivity	High QE & low read noise Global shutter
Fast decision	Low latency	High speed camera	High frame rate
Overexposure & dynamic range	Exposure control, merge images,…	HDR support	High intra-scene dynamic range
No visible flash	3D Stereo-vision, LIDAR, license plate	Near-IR active illuminator	High near-IR QE Global shutter
Resolution & optical format	1” and 2/3” optics (16mm, 11 mm diag)	Megapixels	Pixel size

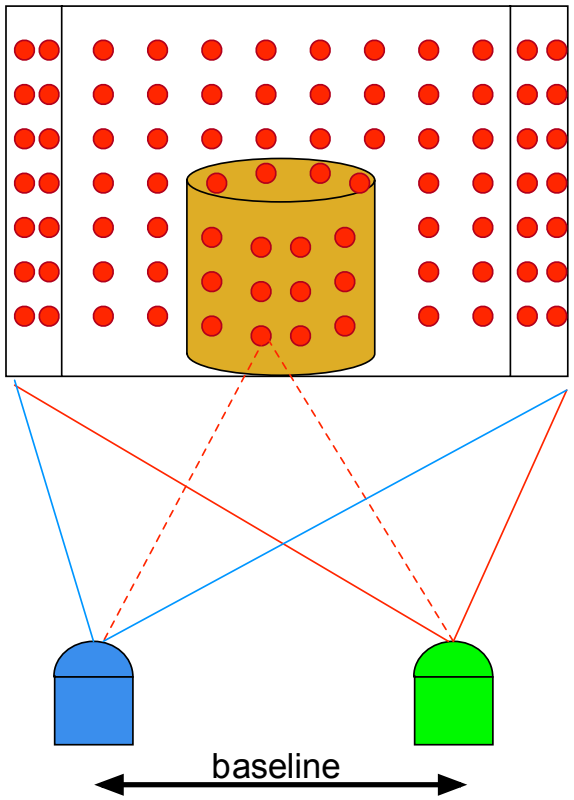
Why global shutter for 3D structured light?

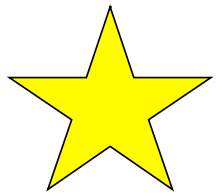


NIR Active illumination 3D imaging

- Structured light – pattern projector
- Calculate depth by triangulation
  - Known baseline
  - Correspondence problem: identify projected pattern in image
  - Recalculate distance

Why global shutter for 3D structured light?

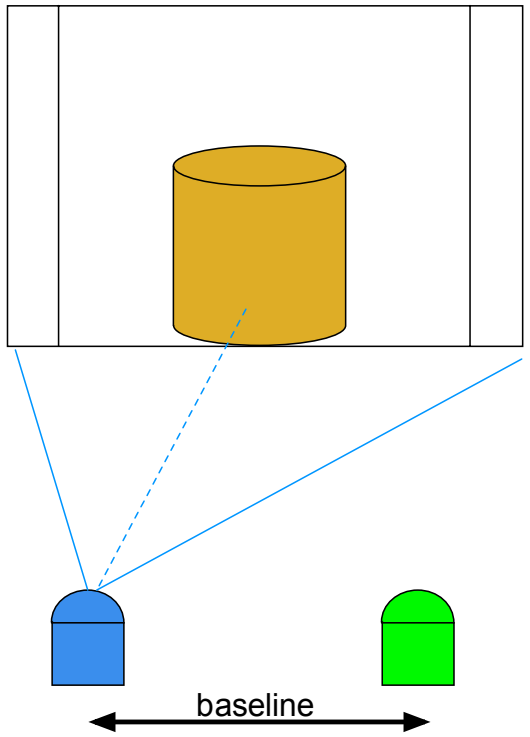


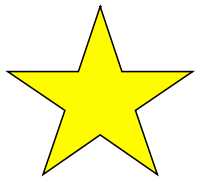


NIR Active illumination

- Illuminator competes against background (sun)light

Global shutter in consumer applications



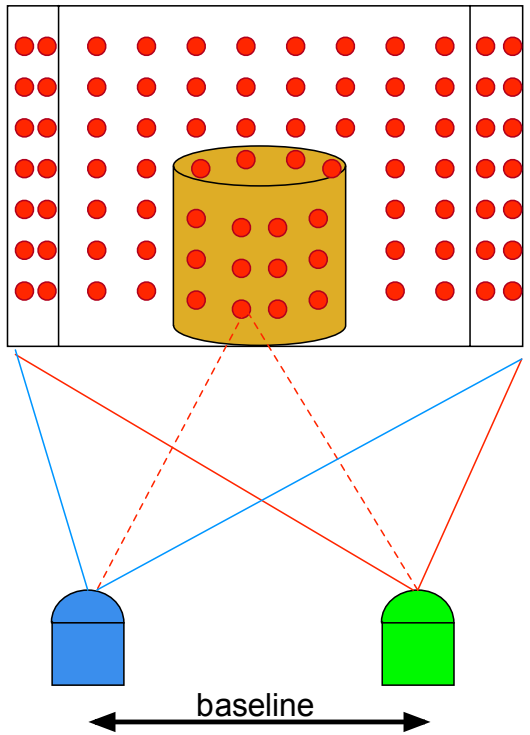


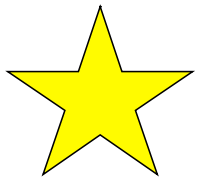
Short intense flash of structured light pattern with synchronized exposure time

Global shutter to suppress signal from background light

Short exposure = little sunlight contribution

Why global shutter for 3D structured light?





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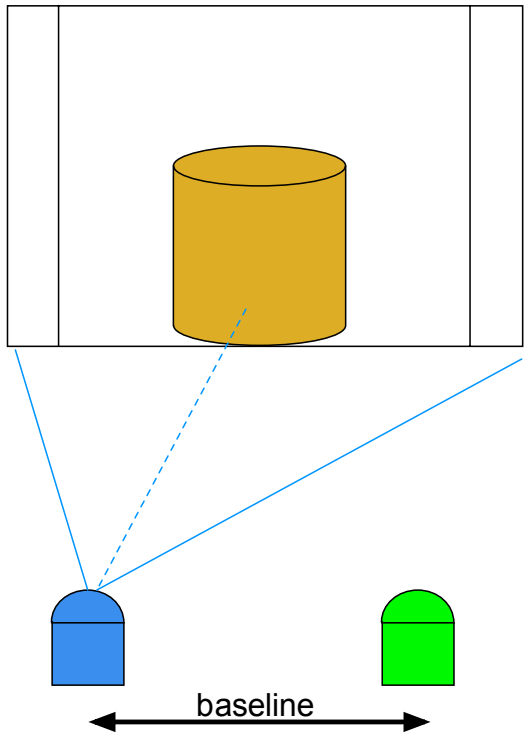
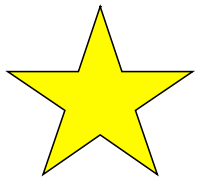




Short intense flash of structured light pattern with synchronized exposure time

Global shutter to suppress signal from background light

Short exposure = little sunlight contribution

Low power consumption in illuminator (short flash)
More intense pulse possible (eye safety limits)

Key requirements for the image sensor

- Global shutter (with good shutter efficiency)
- Low read noise and good dynamic range
- High quantum efficiency, in some cases also for near-IR
- High frame rate
- Small pixel size

Key requirements for the image sensor and solutions

- Global shutter (with good shutter efficiency)
  - IT-CCD -> In-pixel voltage sampling -> In-pixel charge storage -> Voltage sampling with backside illumination
- Low read noise and good dynamic range
  - Correlated double sampling, multiple sampling, column ADC
- High quantum efficiency, in some cases also for near-IR
  - Backside illumination
  - For NIR QE: internal reflections by DTI & scattering structure
- High frame rate
  - Counting ramp column ADCs, Cyclic column ADCs, high bitrate output ch.
- Small pixel size
  - CMOS scaling, pixel architecture, dense capacitors, 3D wafer stacking

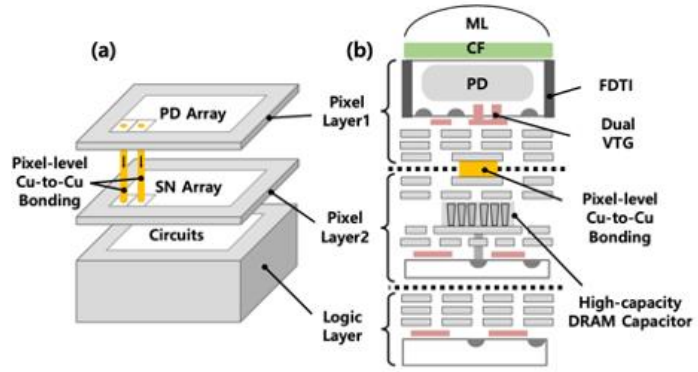
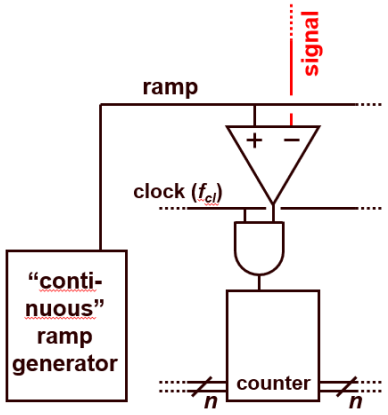


Fig. 2 Cross-section of 3-layer stacked sensor structure



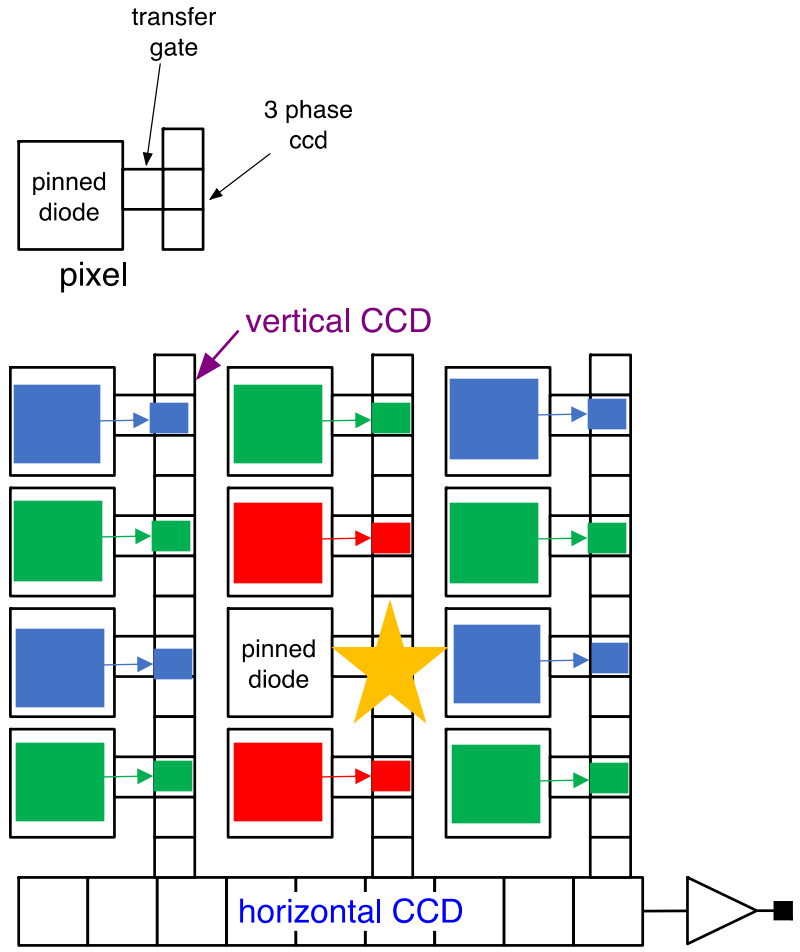
Global shutter image sensor architectures

Interline transfer CCD

- Pinned photodiode (Teranishi, 1982)
- CCD for charge transfer to output stage (V+H)
- Output stage with CDS (low noise)
- Pipelined Global Shutter

Problems:

- Low frame rate (speed)
- No integration of logic
- Photocarriers captured by CCD => smear



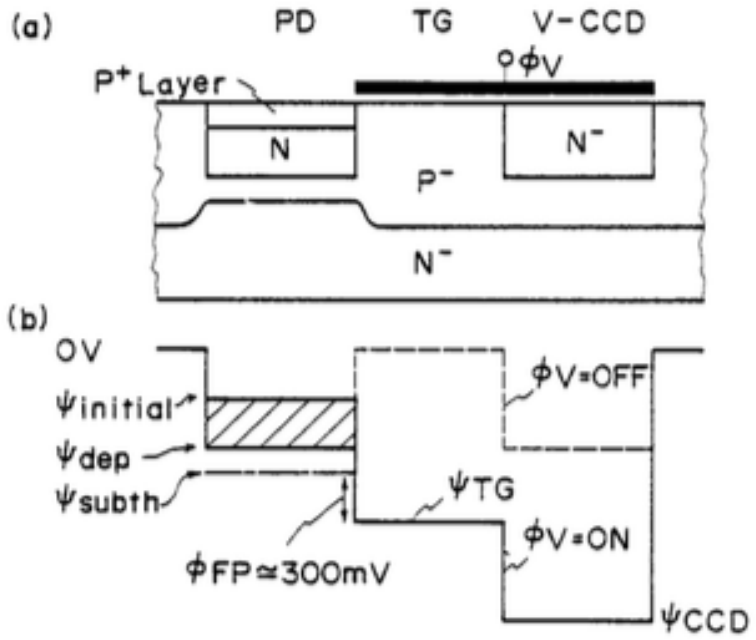


Fig.5. P⁺NP⁻ structure photodiode
(a) Unit cell cross sectional view
(b) Potential profile in a complete transfer mode

N. Teranishi, A. Kohono, Y. ishihara, E. Oda and K. Arai, "No Image Lag Photodiode Structure in the Interline Transfer CCD Image Sensor", proc. IEDM 1982, San Francisco, CA, USA, 1982, pp. 324-327,

Global shutter image sensors

	IT-CCD ~2005
Noise	1-10 e- RMS Trade-off with pixel rate (speed)
QE	Moderate QE Microlenses + waveguides
Frame rate	Low, few fps for Mpixel resolution
Pixel size	~ 3.45 µm

Can we do better?

Easy to improve with CMOS readout

Timeline – global shutter image sensors with CDS

1982: interline transfer CCD

2000-2005: transition CCD->CMOS but not yet for global shutter

2005: in pixel voltage sampling with CDS (expose-then-readout)

2008: in-pixel voltage sampling with CDS and pipelined shutter

2012: in-pixel charge storage

2018: in-pixel charge storage & BSI (Sony)

2022: in-pixel voltage sampling & interconnect (wafer stacking)

In-pixel sampling for CMOS GS pixels with CDS (2005)

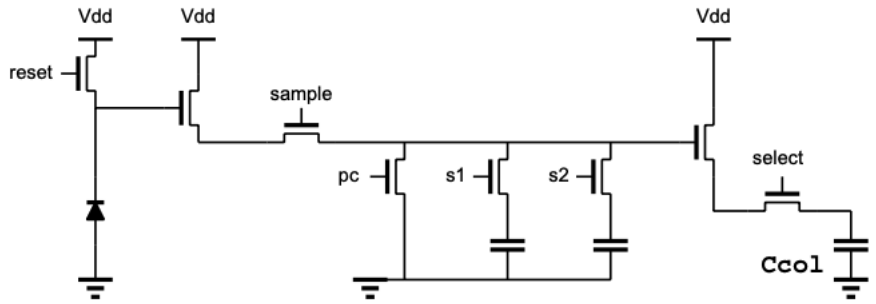
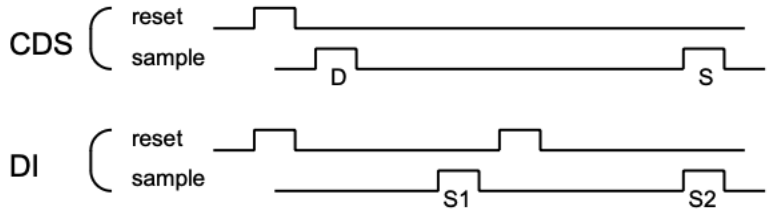


Figure 3: The pixel is a snapshot shutter pixel with two storage capacitors instead of one..

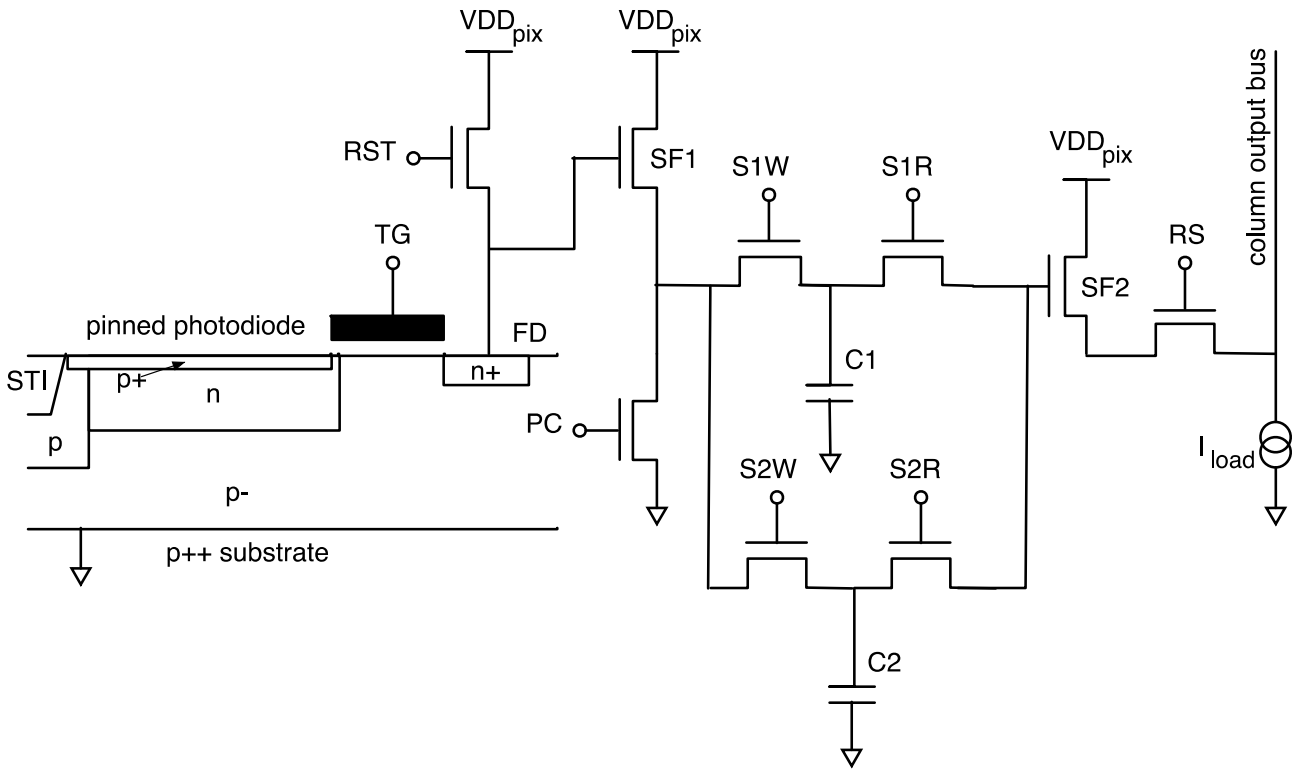


Conversion gain	55	$\mu V/e^-$
Spectral response (@700 nm)	0.12	A/W
Temporal noise (CDS mode)	13	e^-
Dynamic range (CDS mode)	67	dB
Fixed pattern noise (RMS)	0.025	% V_{sat}
Photo response non uniformity	1.1	% (RMS)
Average dark current @20 ^OC	4	mV/s
Common mode rejection ratio	≈ 100	
Reset voltage	4.2	V
Supply voltage	3.3	V
Supply current	40	mA

Acquire, then readout (triggered global shutter)
Long time between reset and signal sample
-> 1/f noise & moderate shutter efficiency

M. Innocent & G.Meynants, “Differential image sensor with high common mode rejection”, Proc. ESSCIRC, Grenoble, France, 2005, pp. 483-486

Voltage domain with CDS



G. Meynants, J. Bogaerts, 2008

Add pinned photodiode & transfer gate

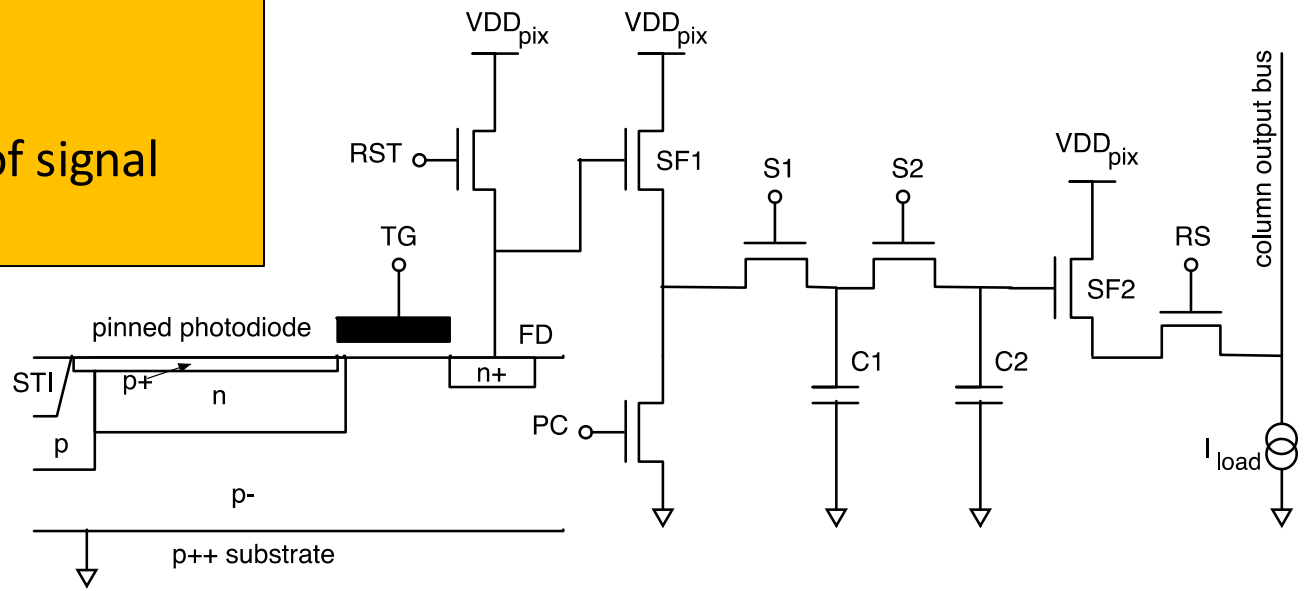
Cancel KTC noise

Good shutter efficiency
(signal on capacitors is common mode)

But large pixel

Smaller with 2 capacitors in series (2009)

2 source followers, 2 storage capacitors
More compact than parallel sample stage
Charge redistribution C1 – C2 → attenuation of signal
Good shutter efficiency (“PLS”), even with BSI

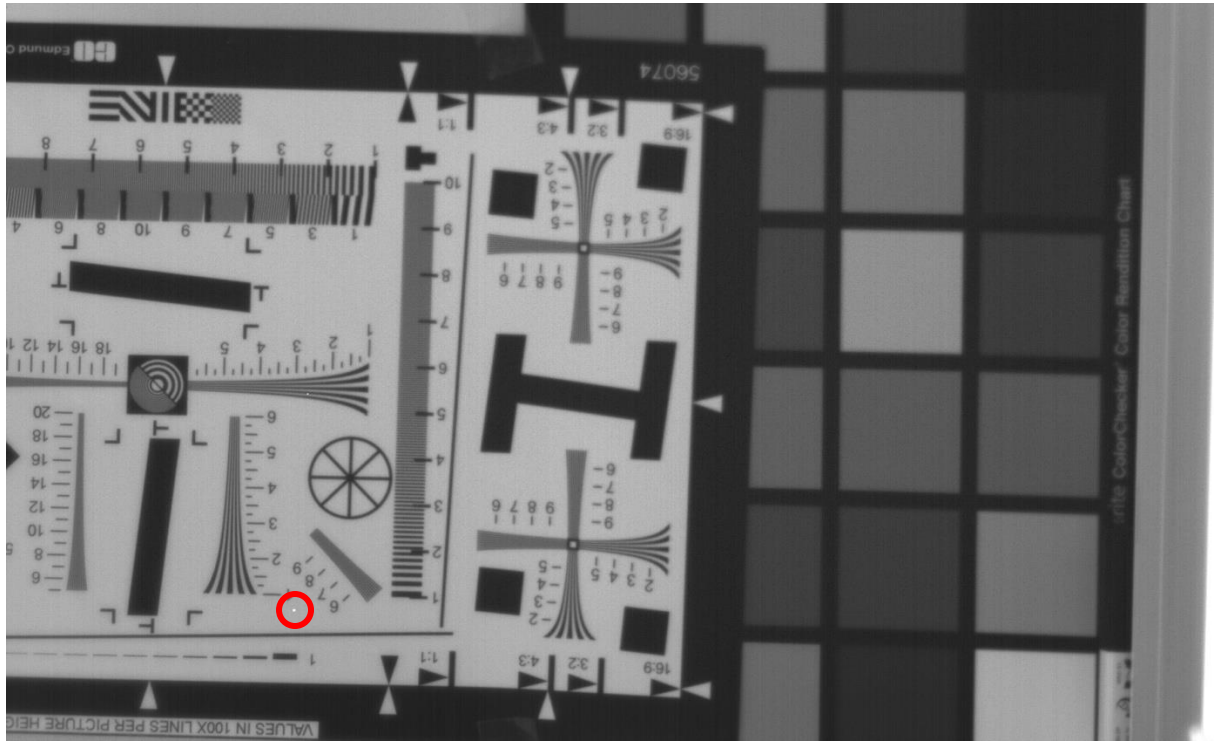


”8T” “hyper-”active pixel

G. Meynants, J. Bogaerts, GB patent application 0806274, 07.04.2008
Xinyang Wang, Jan Bogaerts, Guido Vanhorebeek, Koen Ruythoren, Bart Ceulemans, Gérald Lepage, Pieter Willems, Guy Meynants, “A 2.2M CMOS Image Sensor for High Speed Machine Vision Applications”, proc. SPIE vol. 7536, Jan. 2010

Fig. 1

Backside illuminated global shutter pixel (2011)



Parameter	Value
Pixel size	5.5 µm
Conversion gain	100 µV/e-
Full well charge	13,500 e-
Read noise	10 e- RMS
Dynamic range	62.6 dB
Peak QE	60% (without optimized AR coating) (60% peak frontside illuminated with microlens)
Shutter efficiency Parasitic light sensitivity	99.996% (99.999% on frontside illuminated) 1/25,000 (1/110,000 frontside illuminated)

G. Meynants, Jan Bogaerts, Xinyang Wang, Guido Vanhorebeek, “Backside Illuminated Global Shutter CMOS image sensors”, proc. 2011 International image sensor workshop , 8-11 June 2011

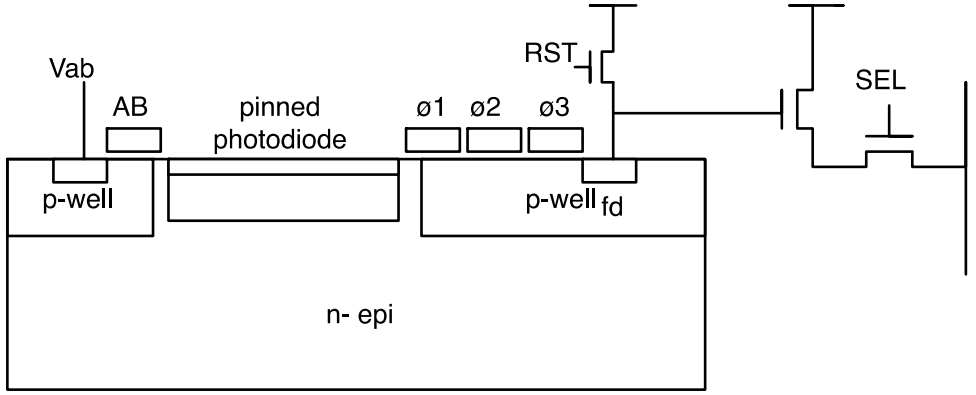
Global shutter image sensors

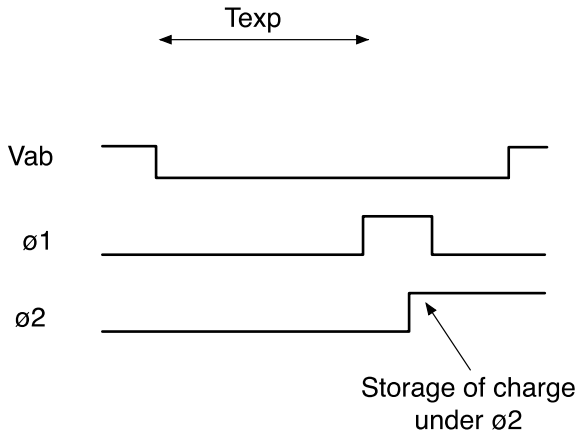
	IT-CCD ~2005	Voltage domain CIS ~2009
Noise	1-10 e- RMS Trade-off with pixel rate (speed)	~ 10 e- RMS
QE	Moderate QE Microlenses + waveguides	= (FSI) > (BSI)
Frame rate	low	300 fps HDTV
Pixel size	~ 3.45 µm	5.5 µm, 3.5 µm (2013)

Can we do better?

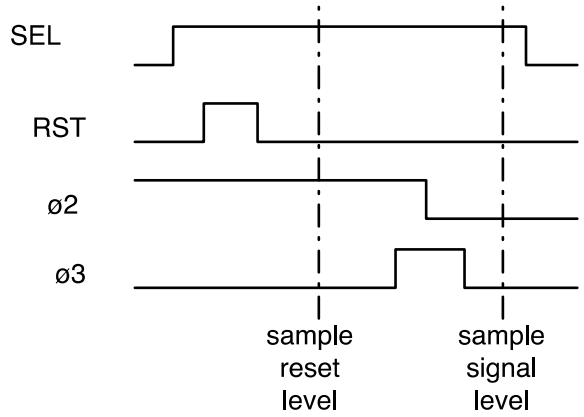
Improve with in-pixel charge storage

Charge domain global shutter pixels



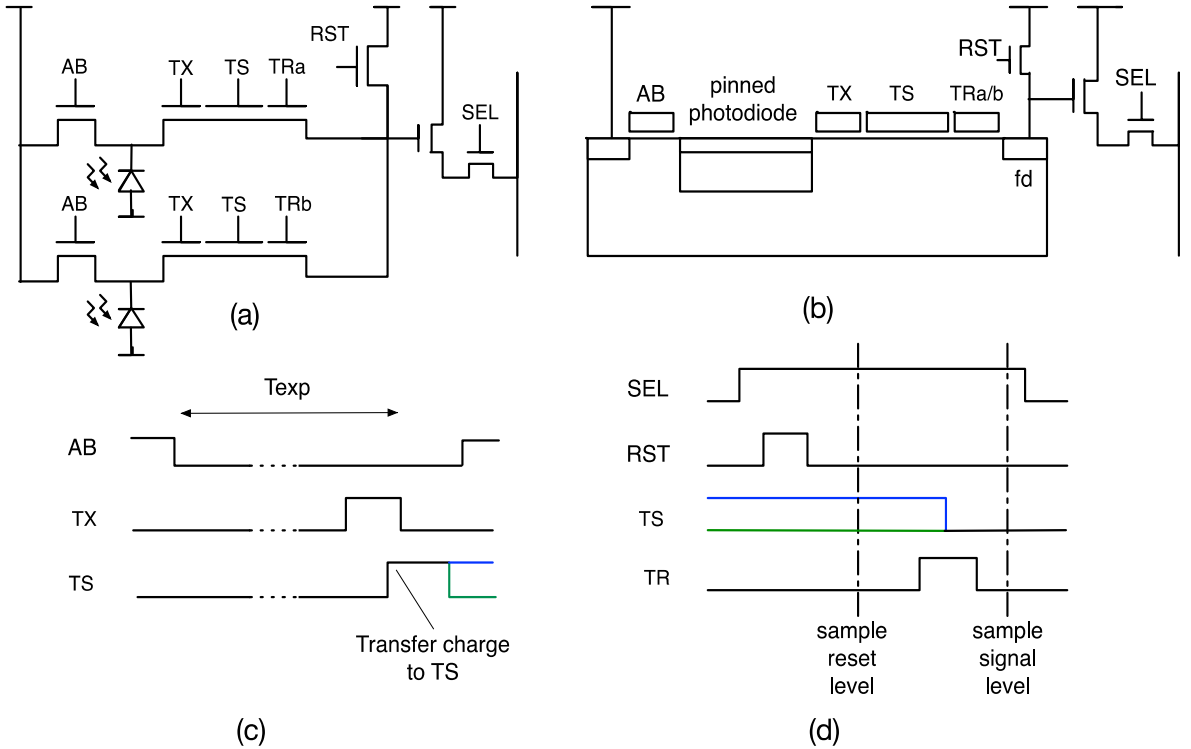


Exposure timing



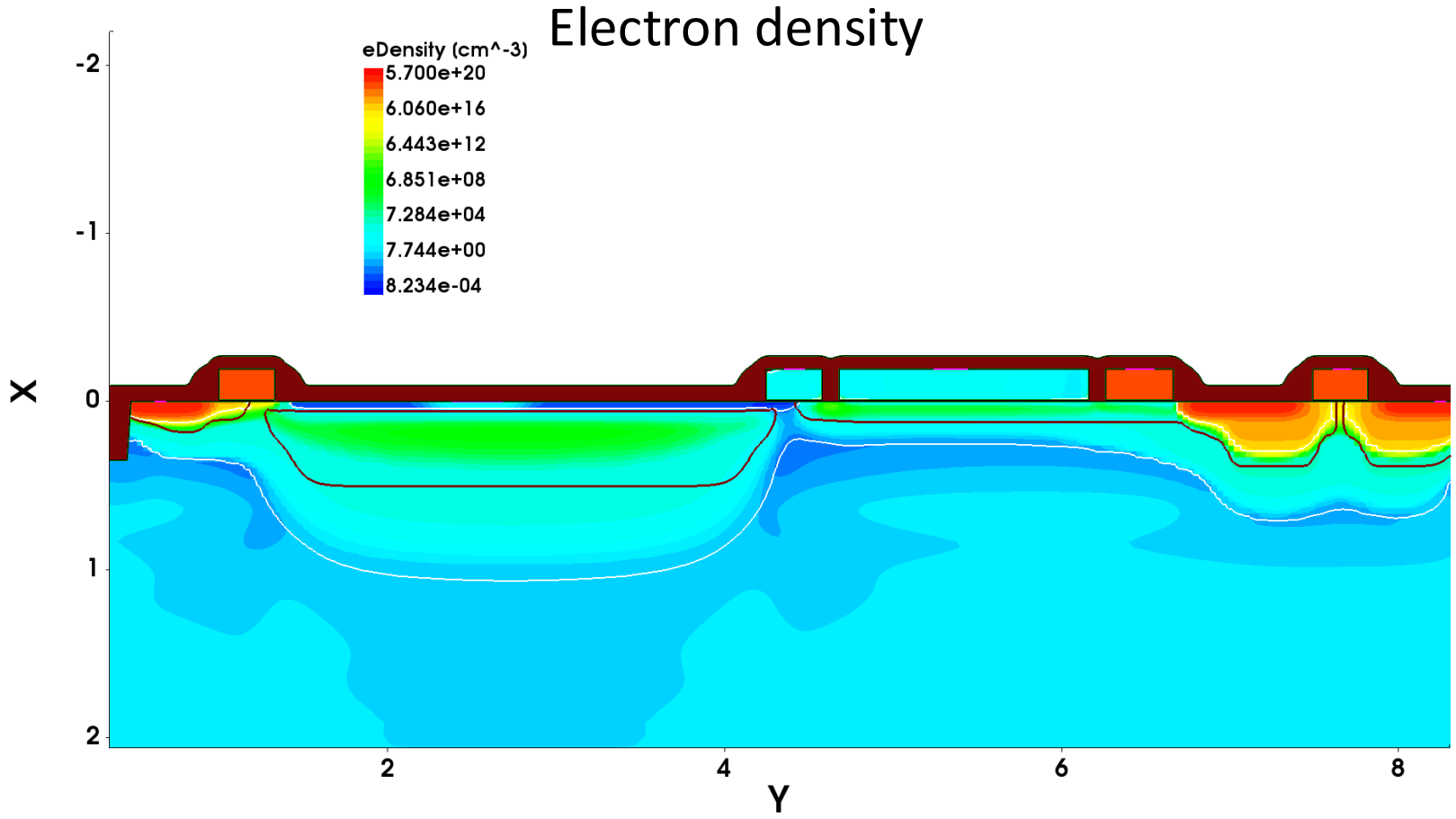
Pixel readout timing

Charge domain global shutter pixels Readout



Close poly spacing (small gap) (thanks to CMOS scaling)

Global shutter pixel – charge transfer to memory and to sense node



Charge domain global shutter (2012)

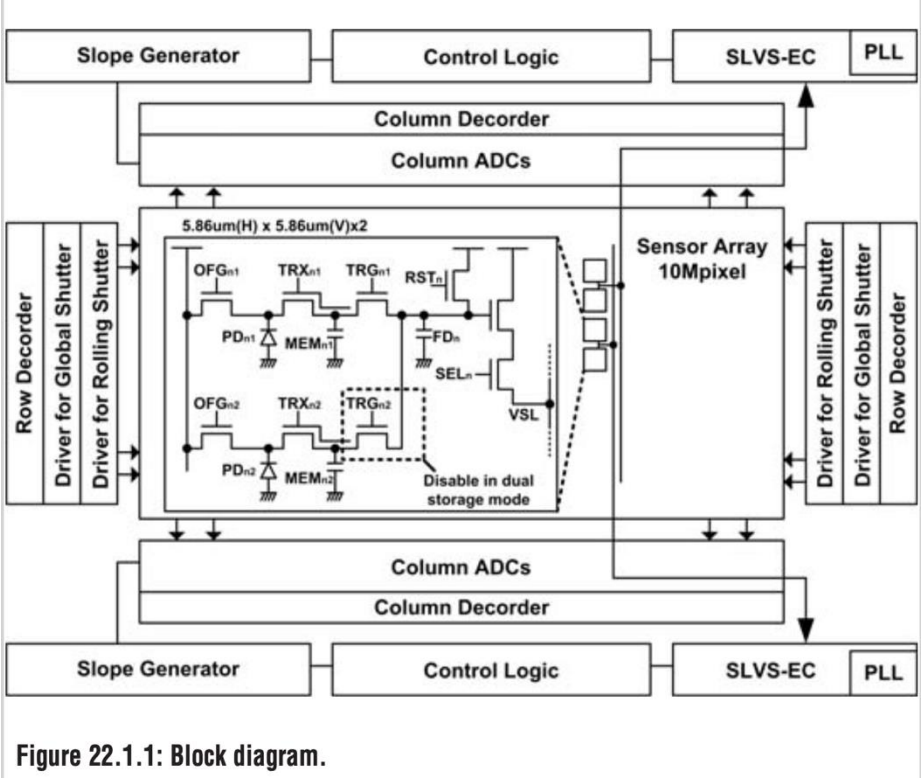


Figure 22.1.1: Block diagram.

Fabrication process	90nm 1P5M + Light Shield
Supply voltage	3.3[V]/1.2[V]/0.4[V]
Effective pixels(Dual-Storage)	5Mpixel
(Single-Storage / Rolling)	10Mpixel
Pixel size	5.86[µm] x 5.86[µm]
Readout rate	30[msec] in Dual-storage mode
Power consumption	2[W]
Saturation signal (Single-Storage)	32200[e-]
(Dual-Storage)	67700[e-]
Sensitivity	78[ke-/lx·s] at 3200K light source with 650nm IR cut-off
Parasitic light sensitivity(MEM / FD)	<-100 [dB]
CDS(MEM) read noise	4.8[e^-_{rms}] (Analog gain +18dB)
Dynamic range (Single-Storage)	76.5[dB]
(Dual-Storage)	83.0[dB]

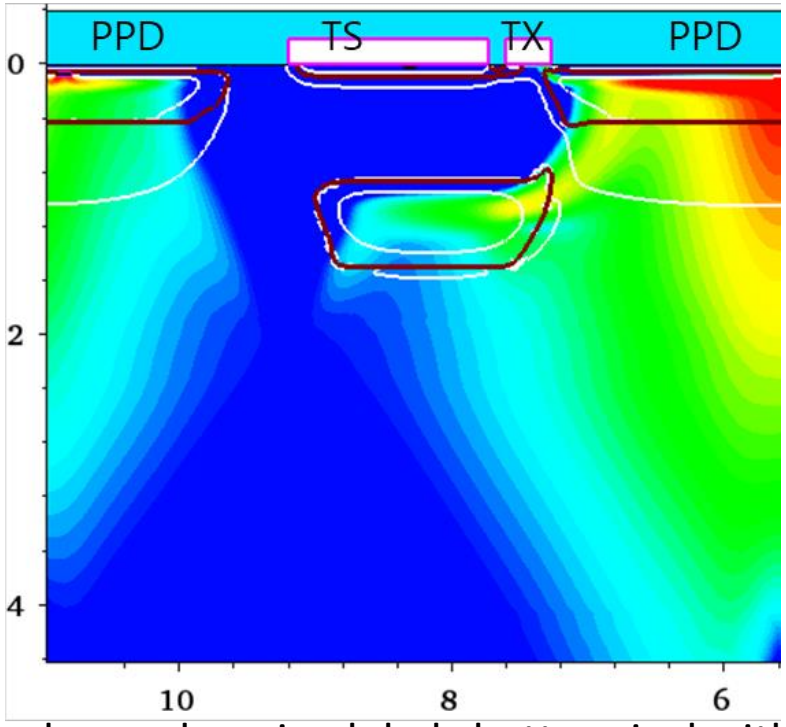
M. Sakakibara, et al, “An 83 dB-Dynamic-Range Single-Exposure Global-Shutter CMOS Image Sensor with in-Pixel Dual Storage”, 2012 ISSCC Digest of Technical Papers, pp. 380-381

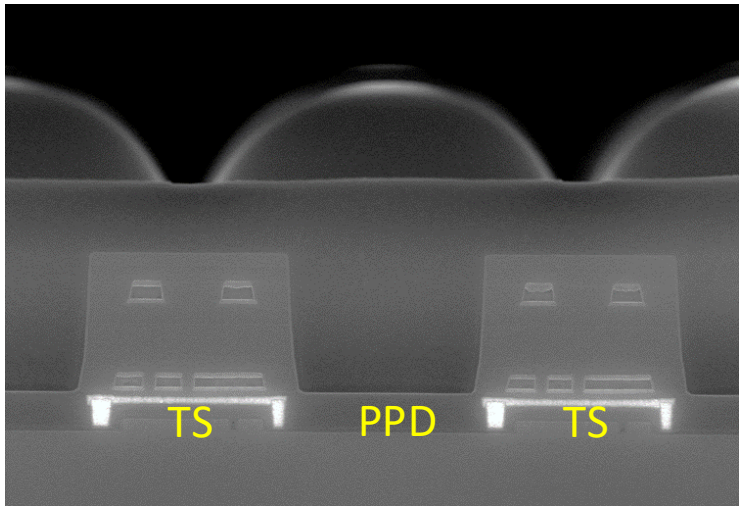
Charge domain global shutter

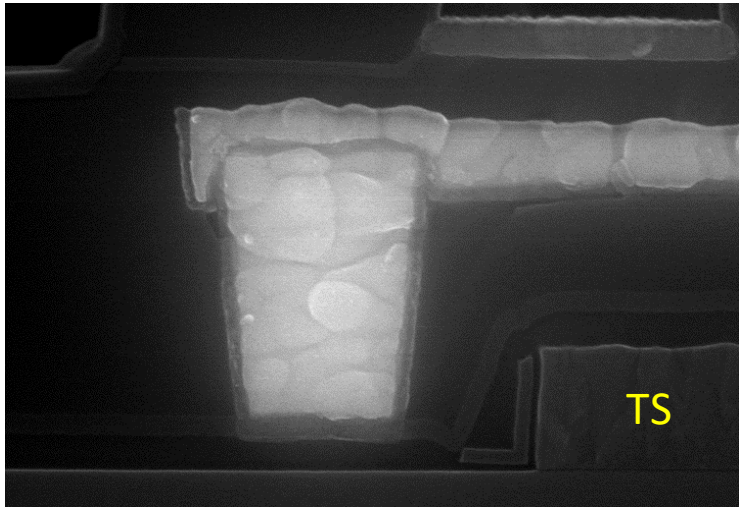
Light shield
Waveguide
} Guide light to photodiode

Implant → e- to PPD

Similar techniques as IT-CCD







G. Meynants, et al, “5.6 µm charge domain global shutter pixel with 90 dB shutter efficiency”, Proc. International Image Sensor Workshop, Sept. 2021

Smaller charge domain global shutter pixel (3.75 µm)

Vertical Storage gate

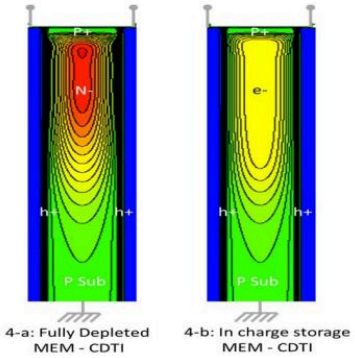
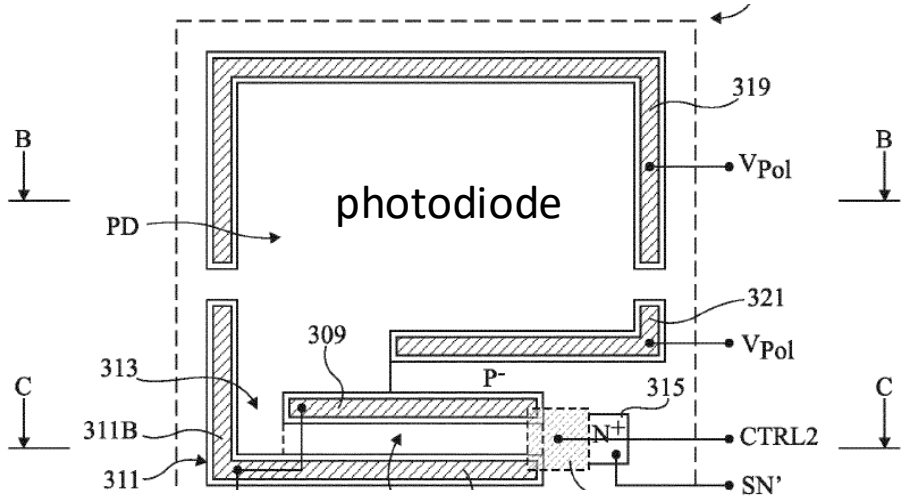


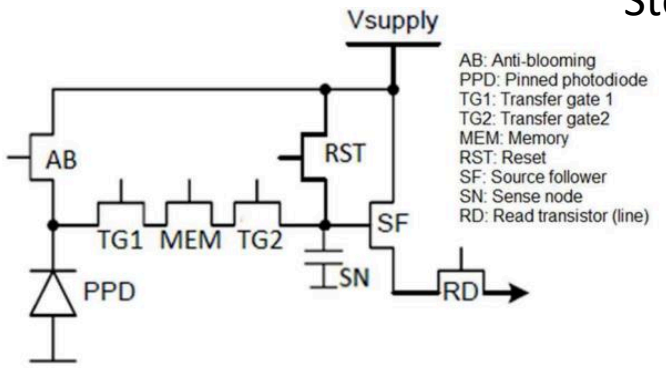
Fig. 4. 2D MEM equipotential lines, 4-a: Empty MEM with Fully depleted N-type zone, 4-b: Full MEM with Neutral N-type zone filed with e-.

TABLE I
PIXEL PERFORMANCES

Characteristics	Value
Pixel Pitch	3.75 µm, 6T Global Shutter
CVF	120 µV/e-
Saturation Charge	12 000 e-
QE @ 550 nm	60%
Sensitivity Mono BG38	17V/lux-s
MEM Dark Current @60°C	25e-/s
PPD Dark Current @60°C	40e-/s
Lag	no lag
Temporal noise floor	2e-
GS Efficiency @ 550nm	99.96%
Dynamic Range	75dB



Storage region



F. Roy, Y. Cazaux, P. Waltz, P. Malinge and N. Billon-Pierron, "Low Noise Global Shutter Image Sensor Working in the Charge Domain," in IEEE Electron Device Letters, vol. 40, no. 2, pp. 310-313, Feb. 2019, doi: 10.1109/LED.2018.2888755.

BSI global shutter: Sony IEDM 2018
"Back-illuminated 2.74 um Pixel Pitch Global Shutter CIS with Charge Domain memory achieving 10ke- Saturation Signal"

Partial deep trenches and through silicon deep trenches increase density of memory charge storage

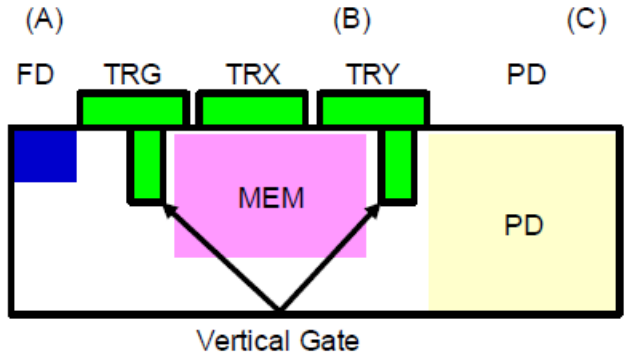


Fig.4 Cross-sectional schematics showing VG along (A) to (C) in Fig.1

Parameter	Value
Process Tecnology	BI 90 nm(BE)/65 nm(FE) 1P4M
Pixel Array	3208 × 2184
Supply Voltage	3.3 V / 1.8V / 1.2V
Pixel Pitch	2.74 μm × 2.74 μm
Color Filter	Monochrome
Dark current @ 60°C,1s,1pix	13.8 e- (PD+MEM)
Temporal Noise	2.00 erms
Full Well Capacity	10000 e-
Sensitivity	23900 e-/lx s (3200K light with IR cut filter)
Parasitic Light Sensitivity	-80 dB
Dynamic Range	74 dB
Quantum Efficiency	85.5 %
Frame Rate	190 fps @ 12bit 260 fps @ 10bit

Charge domain BSI global shutter

Y. Kumagai et al., "Back-Illuminated 2.74 µm-Pixel-Pitch Global Shutter CMOS Image Sensor with Charge-Domain Memory Achieving 10k e-Saturation Signal," 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2018, pp. 10.6.1-10.6.4, doi: 10.1109/IEDM.2018.8614676.

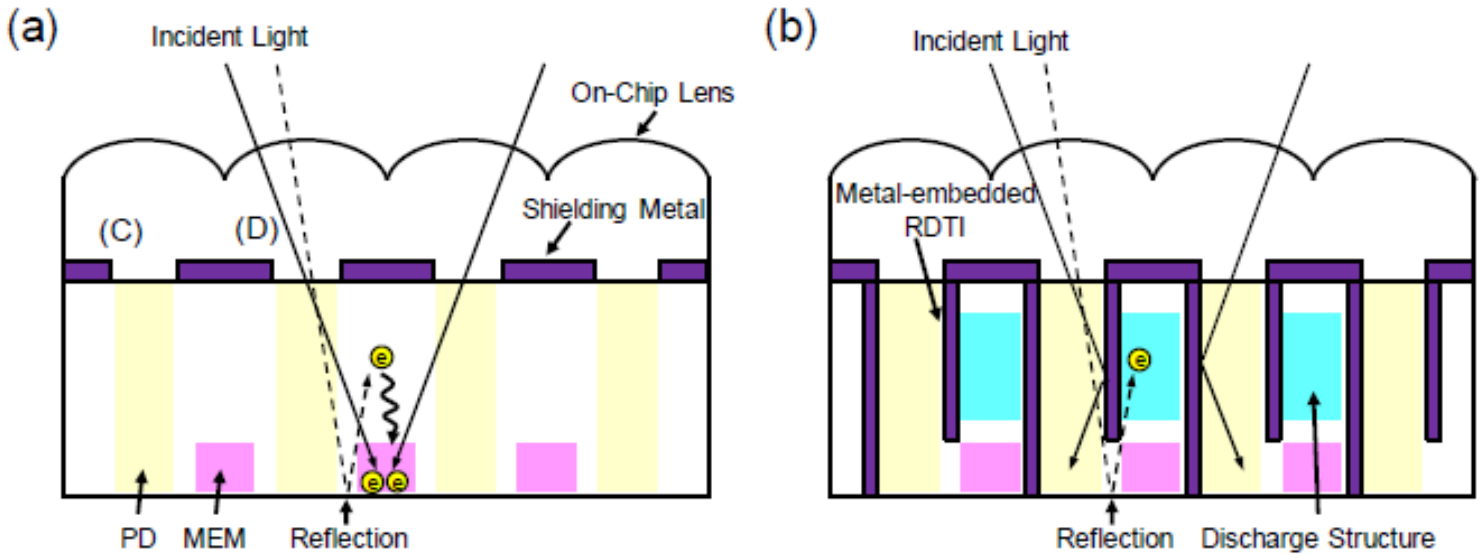


Fig.2 Cross-sectional schematics of back-illuminated GS-CIS with (a) conventional (b) light-shielding structure in this work

Global shutter image sensors

Can we do better?

	IT-CCD ~2005	Voltage domain GS ~2009	Charge domain GS ~ 2012
Noise	1-10 e- RMS Trade-off with pixel rate (speed)	~ 10 e- RMS	2 - 5 e- RMS
QE	Moderate QE Microlenses + waveguides	= (FSI) > (BSI)	= (FSI) > (BSI)
Frame rate	low	high	high
Pixel size	~ 3.45 µm	5.5 µm, 3.5 µm (2013)	3.45 µm 2.74 µm

Improve with wafer stacking & in-pixel interconnect or dense capacitors

Global shutter using 3D wafer stacking with pixel interconnect(1)

IEDM 2022: 1.8 µm voltage domain global shutter pixel (Samsung)

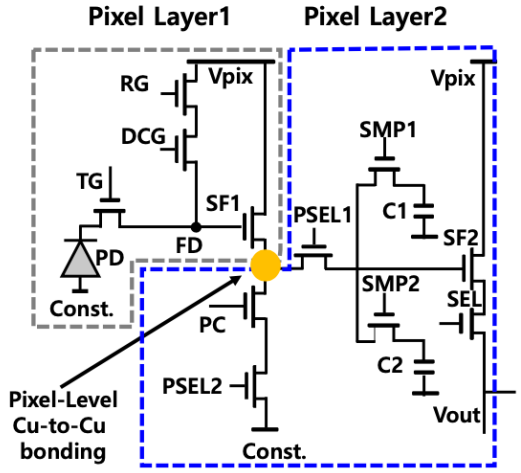


Fig. 1 Circuit schematic of voltage-domain GS pixel

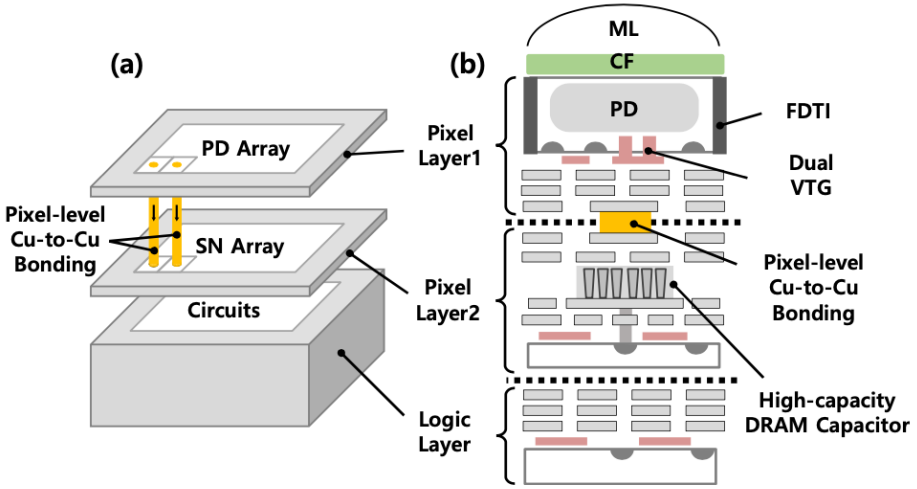


Fig. 2 Cross-section of 3-layer stacked sensor structure

Parameter	Value
Pixel-Pitch	1.8µm x 1.8µm
GS Mode	voltage-domain GS
Procsee Technology	Top 65nm (pixel) Middle 65nm (pixel) Bottom 45nm (logic)
Color Filter	RGB
Supply Voltage	2.8V/1.8V/1.0V
CG (Dual CG operation)	HCG 180µV/e- LCG 60µV/e-
FWC	14000e-@LCG 4600e-@HCG
PLS	<-130dB
Temporal Noise	1.8e-rms @HCG
Dark Current (60C, 1s, 1pix)	6e-
PRNU	0.7%
QE	84%
Sensitivity	11k e-/lux.s (3200k light with IR cut filter)

C1 & C2: 250 fF (DRAM capacitor)

3-Layer Stacked Voltage-Domain Global Shutter CMOS Image Sensor with 1.8µm-Pixel-Pitch

Seung-Sik Kim, Gwi-Deok Ryan Lee, Sang-Su Park, Heesung Shim, Dae-Hoon Kim, Minjun Choi, Sangyoon Kim, Gyunha Park, Seung-Jae Oh, Joosung Moon, Sungbong Park, Sol Yoon, Jihye Jeong, Sejin Park, Sanggwon Lee, HaeJung Lee, Wonoh Ryu, Taehyoung Kim, Doowon Kwon, Hyuk Soon Choi, Hongki Kim, Jonghyun Go, JinGyun Kim, Seunghyun Lim, HoonJoo Na, Jae-kyu Lee, Chang-Rok Moon, and Jaihyuk Song
Samsung Electronics, Hwaseong, Korea, email: seungsik.kim@samsung.com

Samsung

Global shutter: using 3D wafer stacking with pixel interconnects (2)

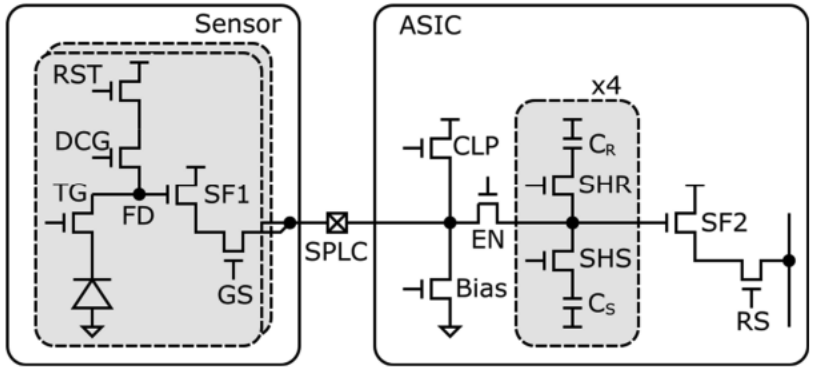
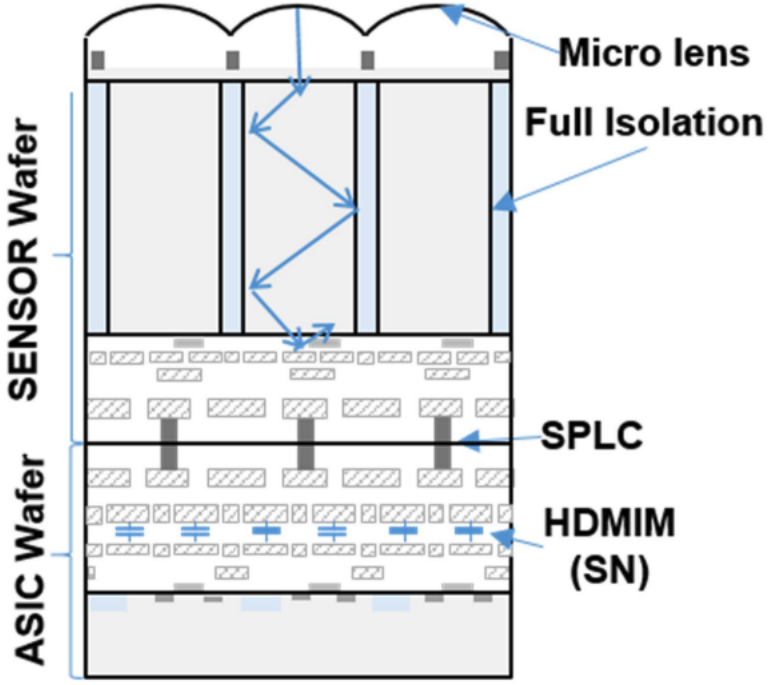


Fig. 1. Circuit schematic of the proposed voltage domain global shutter pixel.

Parameter	Value
Pixel array pitch	2.2µmx2.2µm
GS Mode	V-domain
Process Technology	TSMC 45n CIS/65n logic stacked BSI
Color Filter	Monochrome
CG	Dual CG : 60/200 µV/e-
FWC	3500 e-/11000 e-
Effective Shutter efficiency @940nm	>100dB
RN	3.8 e-
FPN	1.2 e-
DC	25 e-/s @ 60°C
PRNU@940nm	0.6%
QE @940nm QE @850nm	38% 53%
MTF@940nm, Ny/2	60% on Axis, 57%@30°

Table 1. Pixel performance summary.

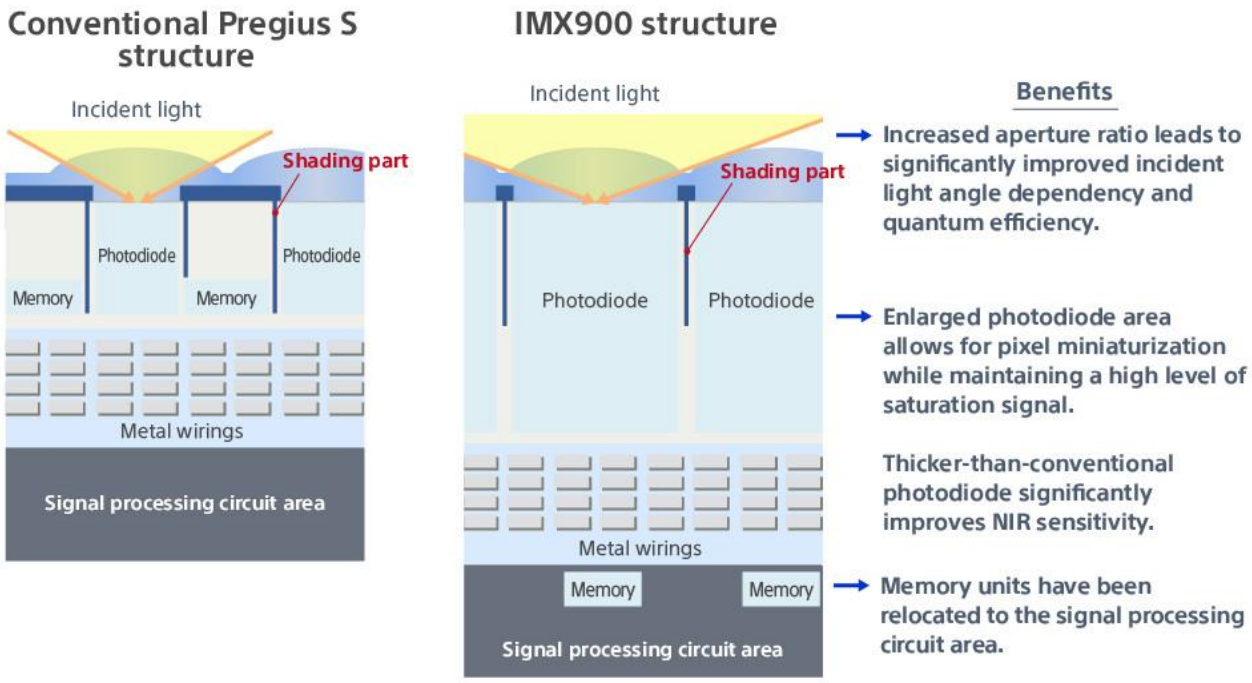


g. 2. Schematic cross section of stacked structure illustrating the sensor pixel and SN arrays.

Omnivision

Z. Gao, et al, “A 2.2 µm 2-Layer Stacked HDR Voltage Domain Global Shutter CMOS Image Sensor with Dual Conversion gain and 1.2 e- FPN”, proc. 2023 IEDM, Dec. 2023, p. 40-2

Sony wafer stacked 2.25 µm GS (IMX900) voltage domain?



From Sony press release 25 oct 2023 (announcement IMX9000 3.2MPixel with 2.25 µm global shutter)
https://www.sony-semicon.com/en/products/is/industry/gs/imx900.html

ST voltage domain GS in single pixel layer

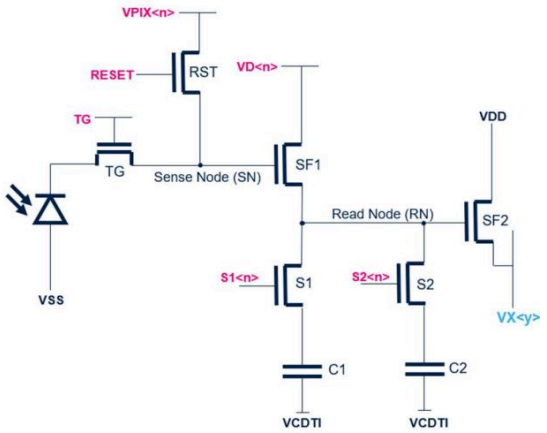


Fig. 1. Pixel schematic

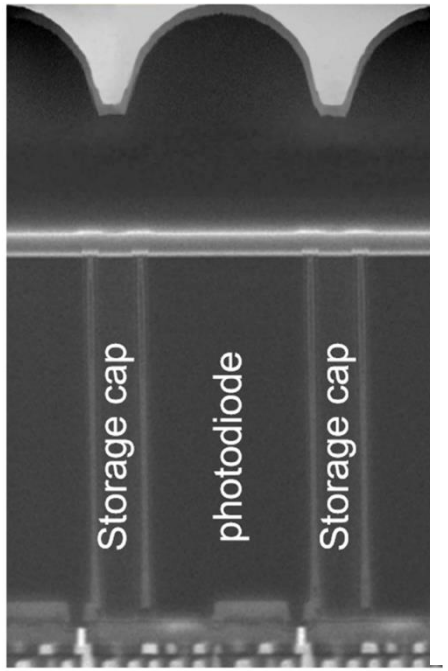


Fig. 3. SEM cross-section view of the pixel. Cut done in diagonal in the micro lens's corner.

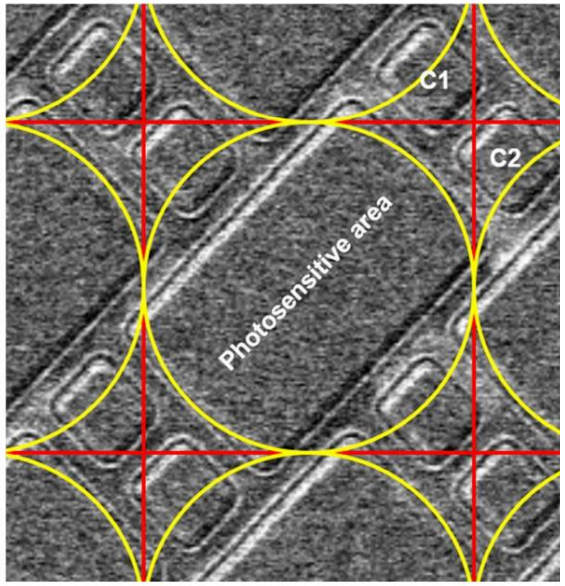


Fig. 5. Pixel CDTI top view. Micro lens footprints are indicated in ye

	Pixel performance at 60C
Pixel pitch (µm)	2.16
Pixel architecture	6T-2C single layer VDGS
Array size	804 x 704
Die size (mm²)	2.75 x 2.17
Technology node	Imager 65nm + logic 40nm
Full well (e-)	7000
PRNU @ 2ke-	0.7%
Idark PD (e-/s)	10
Idark Retention (e-/s)	25
TN (e-)	4.3
PLS at 940nm	-90dB
QE at 940nm	23%
MTF @ Nyquist/2	0.53

Table I. Pixel performance summary

55 fF/µm²

P. Maligne, et al, "2.16 µm Backside illuminated Voltage domain Global Shutter CMOS image Sensor with single silicon layer pixel", proc. IEDM 2023,

Global shutter image sensors

	IT-CCD ~2005	Voltage domain GS ~2009	Charge domain GS ~ 2012	Voltage domain ~ 2024
Noise	1-10 e- RMS Trade-off with pixel rate (speed)	~ 10 e- RMS	2 - 5 e- RMS	~ 4 e-
QE	Moderate QE Microlenses + waveguides	= (FSI) > (BSI)	= (FSI) > (BSI)	> (BSI)
Frame rate	low	high	high	high
Pixel size	~ 3.45 µm	5.5 µm, 3.5 µm (2013)	3.45 µm 2.74 µm	~2.2 µm

What's next?

Are smaller global shutter pixels still needed?

Should frame rate further increase?

Or is it more useful to make our pixels more functional?

Can pixel level optics bring extra functionality?

Should the spectral range of wavelengths be extended?

Should the pixel array be addressed in a smarter way?

Should the pixel be more intelligent in the era of machine vision with artificial intelligence?

Should we further investigate in-pixel circuit options to detect changes or local features inside or closer to the pixel matrix?

What’s next? Is AI changing the needs?

Are smaller global shutter pixels still needed?

Should frame rate further increase?

Or is it more useful to make our pixels more functional?

Can pixel level optics bring extra functionality?

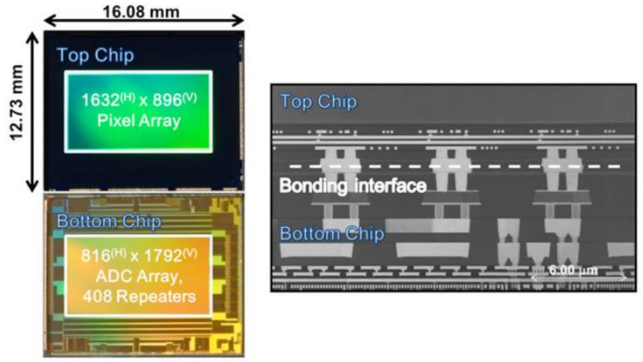
Should the spectral range of wavelengths be extended?

Should the pixel array be addressed in a smarter way?

Should the pixel be more intelligent in the era of machine vision with artificial intelligence?

Should we further investigate in-pixel circuit options to detect changes or local features inside or closer to the pixel matrix?

More functionality in the pixel. ADC



In-pixel ADC, 1.46 Mpixel, 660 fps, 14 bit, 70 dB, 746 mW

Sony, ISSCC 2018

5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC

Masaki Sakakibara[1], Koji Ogawa[1], Shin Sakai[1], Yasuhisa Tochigi[1], Katsumi Honda[1], Hidekazu Kikuchi[1], Takuya Wada[1], Yasunobu Kamikubo[1], Tsukasa Miura[1], Masahiko Nakamizo[1], Naoki Jyo[2], Ryo Hayashibara[2], Yohei Furukawa[3], Shinya Miyata[3], Satoshi Yamamoto[1], Yoshiyuki Ota[1], Hirotsugu Takahashi[1], Tadayuki Taura[1], Yusuke Oike[1], Keiji Tatani[1], Takashi Nagano[1], Takayuki Ezaki[1], Teruo Hirayama[1]

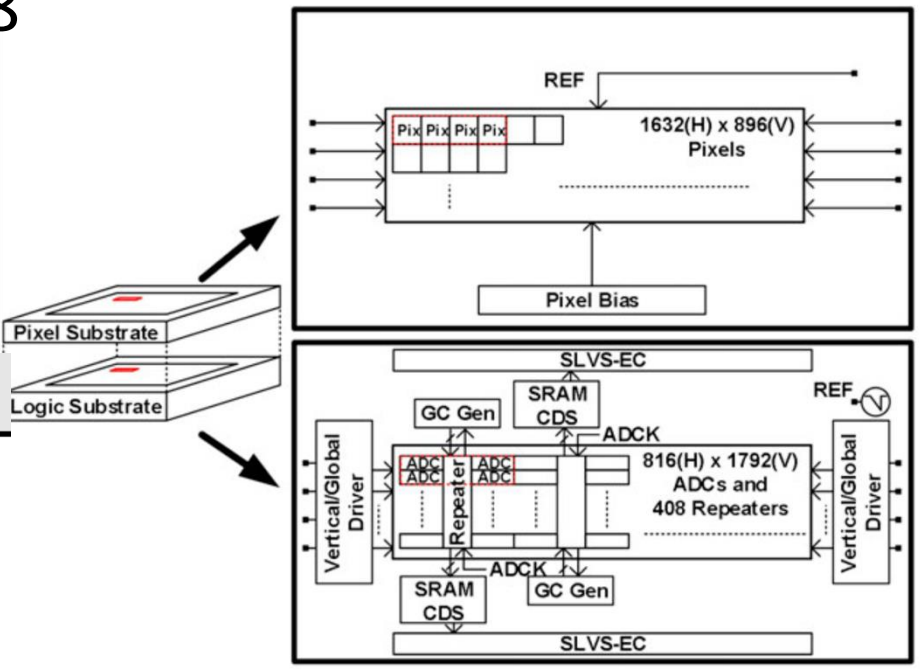


Figure 5.1.1: Simplified block diagram of pixel-parallel ADC.

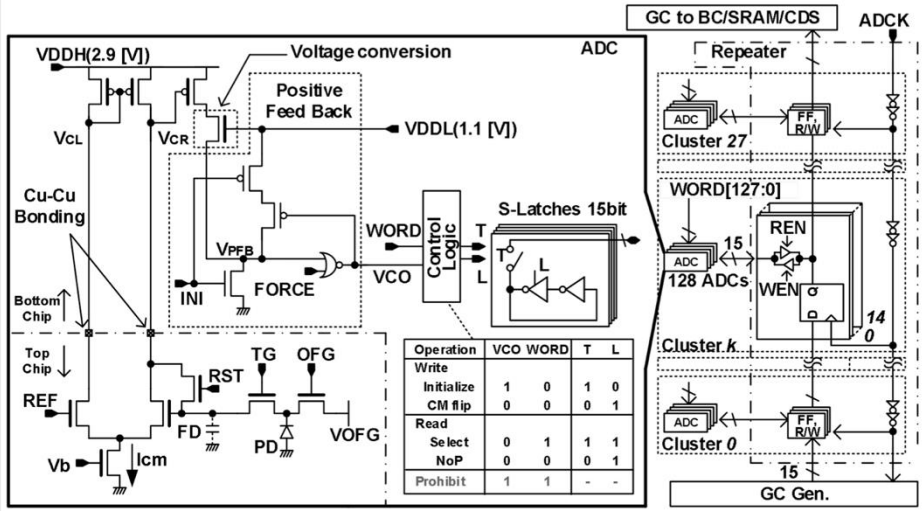


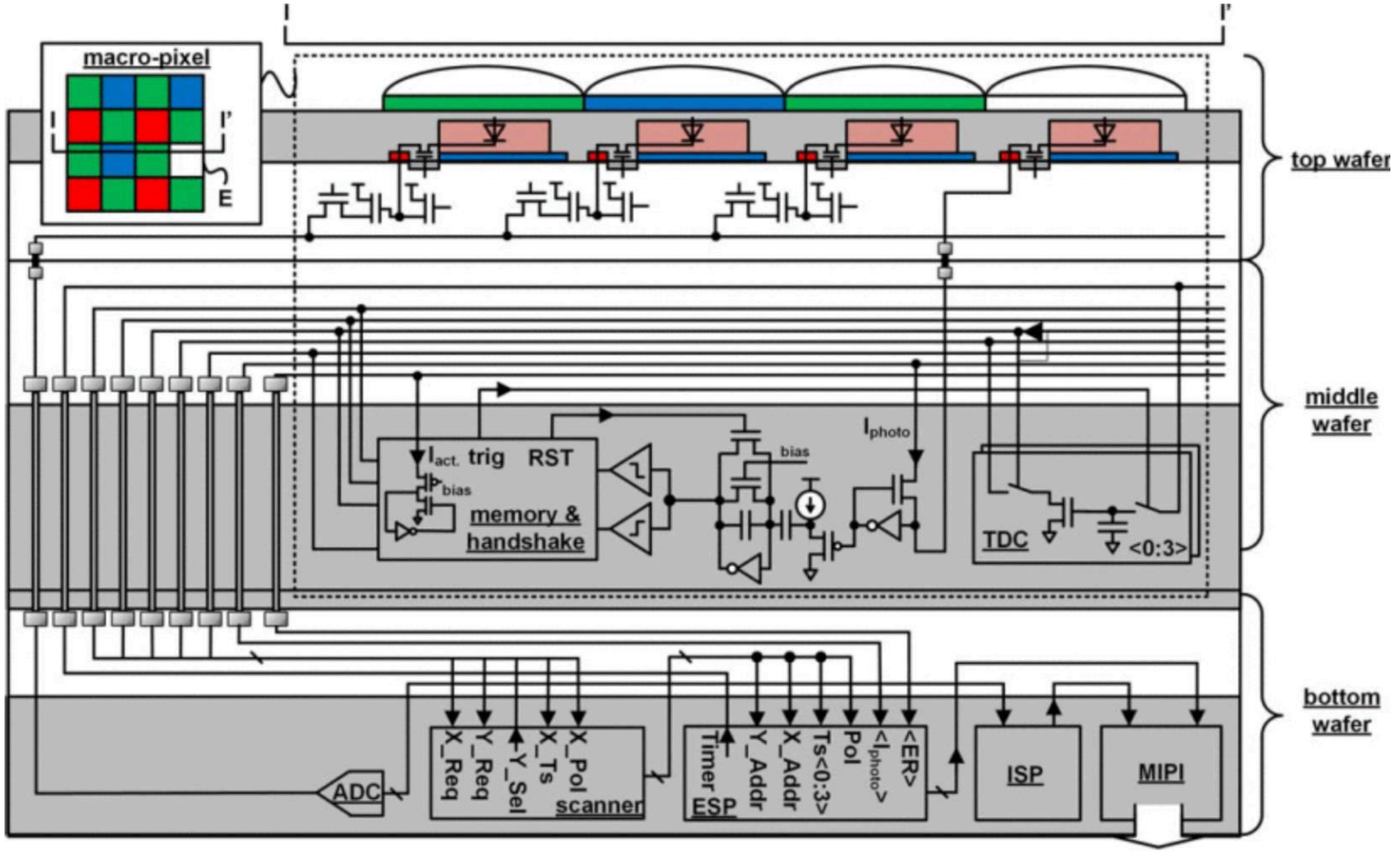
Figure 5.1.2: Simplified circuit schematic of pixel-parallel ADC and block diagram of repeater.

Event-driven pixels

- 1989 C. Mead, M. Mahowald “Analog VLSI and Neural Systems”, Chapter 15 “Silicon Retina”
- T. Delbrück, ETH Zurich, bio-inspired and neuromorphic event-based image sensors and processing, many event-driven imagers and event vision sensors
- Prophesee, Sony, Omnivision, Samsung

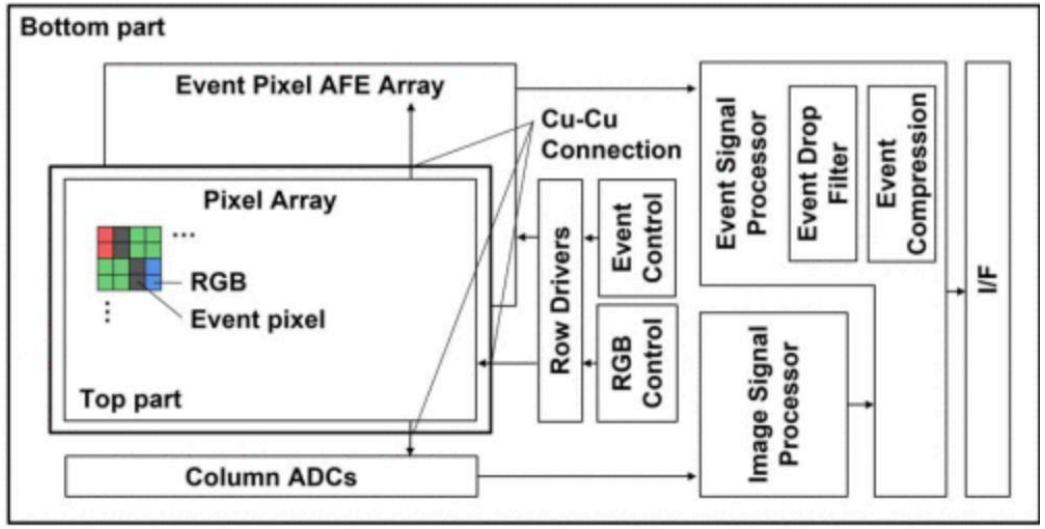
Example EVS Omnivision

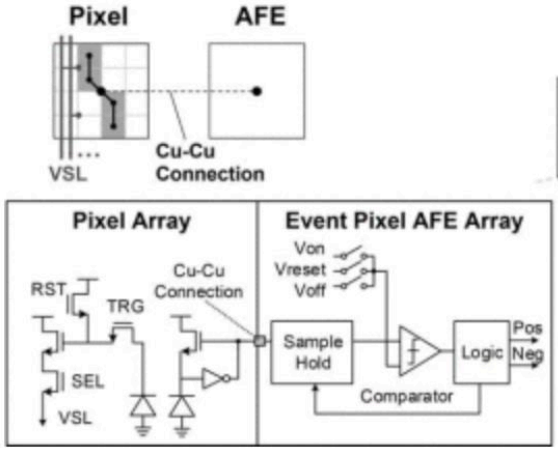
EVS pixel -> log amplifier -> contrast detecting filter -> contrast change threshold -> latch and TDC

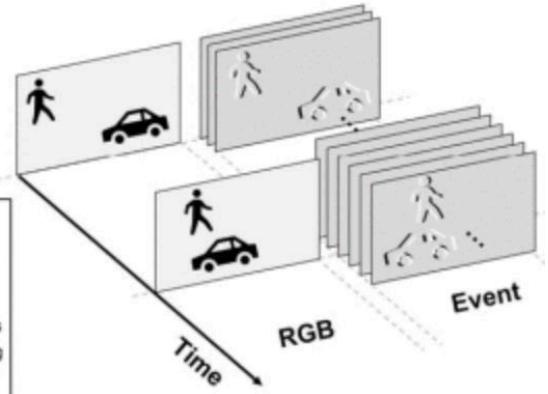


M. Guo *et al.*, "A 3-Wafer-Stacked Hybrid 15MPixel CIS + 1 MPixel EVS with 4.6GEvent/s Readout, In-Pixel TDC and On-Chip ISP and ESP Function," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 90-92, doi: 10.1109/ISSCC42615.2023.10067476

Example EVS (2) Sony



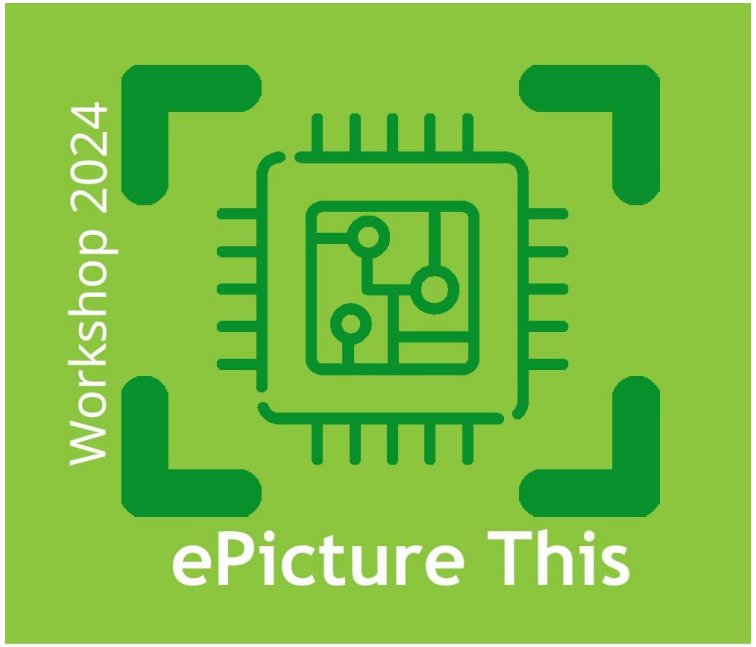




K. Kodama *et al.*, "1.22µm 35.6Mpixel RGB Hybrid Event-Based Vision Sensor with 4.88µm-Pitch Event Pixels and up to 10K Event Frame Rate by Adaptive Control on Event Sparsity," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 92-94, doi: 10.1109/ISSCC42615.2023.10067520.

Conclusions

- Machine vision needs image sensors with dedicated specifications
- New architectures have popped up over the years, thanks to continued architectural innovations, technology advancements (like BSI and 3D stacking) and semiconductor scaling
- What's next? Promising technologies are on the horizon once again



THANK YOU

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